TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No.
END920010133US1

In Re Application Of: **Eric A. Johnson, et al.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/692,921	October 24, 2003	Derek L. Dupuis	23389	2883	9037

Invention: **PASSIVE ALIGNMENT OF VSCELs TO WAVEGUIDES IN OPTO-ELECTRONIC CARDS AND PRINTED CIRCUIT BOARDS**

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Dated: **March 17, 2006**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Eric A. Johnson, et al.

Examiner: Derek L. Dupuis

Serial No: 10/692,921

Art Unit: 2883

Filed: October 24, 2003

Docket: END920010133US1 (15171)

For: PASSIVE ALIGNMENT OF VSCELs TO WAVEGUIDES IN OPTO-ELECTRONIC CARDS AND PRINTED CIRCUIT BOARDS

Dated: March 17, 2006

Confirmation No.: 9037

Hon. Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

Pursuant to 35 U.S.C. 134 and 37 C.F.R. 41.37, entry of this Appeal Brief in support of the Notice of Appeal filed January 17, 2006 in the above-identified patent application is respectfully requested.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Hon. Commissioner for Patents, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450, on March 17, 2006.

Dated: March 17, 2006

Leopold Presser

I. Statement of Real Party in Interest

The real party interest in the above-identified patent application is the International Business Machines Corporation.

II. Statement of Related Appeals and Interferences

There are no other prior or pending appeals, interferences or judicial proceedings known to appellants, the appellants' legal representative, or assignee which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. Statement of Claim Status and Appealed Claims

A. Claim Status

Claim 1 stands rejected based on 35 U.S.C. 102(e) and U.S. Patent No. 6,834,133 B1, and is objected to on an informality.

Claim 2 stands rejected based on 35 U.S.C. 103(a), as being unpatentable over U.S. Patent No. 6,834,133 B1, in view of U.S. Publication No. 2005/0105860 A1

Claim 3 has been cancelled.

Claim 4 has been cancelled.

Claim 5 stands rejected based on 35 U.S.C. 103(a), as being unpatentable over U.S. Patent No. 6,834,133 B1, in view of U.S. Patent Publication No. 2002/00084522 A1.

Claim 6 stands rejected based on 35 U.S.C. 103(a), as being unpatentable over U.S. Patent No. 6,834,133 B1, in view of U.S. Patent Publication No. 2002/00084522 A1.

Claim 7 stands rejected based on 35 U.S.C. 103(a), as being unpatentable over U.S. Patent No. 6,834,133 B1, in view of U.S. Patent Publication No. 2002/00084522 A1.

Claim 8 stands rejected based on 35 U.S.C. §102(e) and U.S. Patent No. 6,834,133 B1.

Claim 9 stands rejected based on 35 U.S.C. 103(a), as being unpatentable over U.S. Patent No. 6,834,133 B1, in view of U.S. Publication No. 2005/0105860 A1.

Claim 10 stands rejected based on 35 U.S.C. 103(a), as being unpatentable over U.S. Patent No. 6,834,133 B1, in view of U.S. Publication No. 2005/0105860 A1.

Claim 11 stand rejected based on 35 U.S.C. 102(e) and U.S. Patent No. 6,834,133 B1, and is objected to on an informality.

Claim 12 stands rejected based on 35 U.S.C. 103(a), as being unpatentable over U.S. Patent No. 6,834,133 B1, in view of U.S. Publication No. 2005/0105860 A1.

Claim 13 has been cancelled.

Claim 14 has been cancelled.

Claim 15 stands rejected based on 35 U.S.C. 103(a), as being unpatentable over U.S. Patent No. 6,834,133 B1, in view of U.S. Patent Publication No. 2002/00084522 A1.

Claim 16 stands rejected based on 35 U.S.C. 103(a), as being unpatentable over U.S. Patent No. 6,834,133 B1, in view of U.S. Patent Publication No. 2002/00084522 A1.

Claim 17 stands rejected based on 35 U.S.C. 103(a), as being unpatentable over U.S. Patent No. 6,834,133 B1, in view of U.S. Patent Publication No. 2002/00084522 A1.

Claim 18 stands rejected based on 35 U.S.C. 102(e) and U.S. Patent No. 6,834,133 B1.

Claim 19 stands rejected based on 35 U.S.C. 103(a), as being unpatentable over U.S. Patent No. 6,834,133 B1, in view of U.S. Publication No. 2005/0105860 A1.

Claim 20 stands rejected based on 35 U.S.C. 103(a), as being unpatentable over U.S. Patent No. 6,834,133 B1, in view of U.S. Publication No. 2005/0105860 A1.

Claims 21-23 have been withdrawn from consideration.

B. Appealed Claims

Claims 1, 2, 5-12 and 15-20 are appealed. A clean copy of these claims is appended in Appendix A to this Appeal Brief.

IV. Statement of Amendment Status

No amendments are pending in this application. The last Amendment filed in this case was dated September 2, 2005. That Amendment was entered.

V. Summary of Claimed Subject Matter

The present invention, as defined by the appealed claims, relates to a method of producing opto-electronic cards and printed circuit boards which are adapted to provide for the passive alignment of VCSELs to waveguides (Page 1, Paragraph [0001], Lines 1 to 3, Page 5, Paragraph [0019]). Moreover, the invention relates to opto-electronic cards and printed circuit boards which incorporate structure providing for the passive alignment of VCSELs to waveguides (Page 1, Paragraph [0001], Lines 3 to Page 5, Paragraph [0021]).

Basically, as indicated in the specification, optical waveguides operate with higher ranges of bandwidths than copper circuits which are employed in printed circuit boards, consequently requiring essentially less operating power, while also not being as susceptible to so-called cross-talk which is encountered in such types of printed circuit boards. Ordinarily, in the technology, waveguides have been utilized in connection with transmissions taking place over long distances; however, more recently, as a result of decreasing manufacturing costs and due to the high bandwidths which are achievable with VCSELs (Vertical Cavity Surface Emitting Lasers), such optical waveguides are increasingly employed in LANs (Local Area Networks). These optical waveguides are currently being used to communicate between processor boards, among other applications in industry and commerce.

The invention, as described, is directed to the obtaining of an improved passive alignment between VCSELs or PIN arrays and waveguides within electronic built-up layers of opto-electronic packages (Page 7, Paragraph [0027]). Moreover, the thermal stability of the applicable opto-electronic card or printed circuit board (PCB) may be considerably improved through the employment of a core constituted of a low expansion material mounting the optical components and a first built-up layer, as a consequence of which the accommodation of larger VCSELs and PIN arrays, as well as the use of smaller waveguide dimensions can be readily rendered possible so as to enhance the versatility and economic efficacy of the present invention (Page 7, Paragraph [0028]).

Pursuant to the invention (Page 7, Paragraph [0029]), the extent of precision of alignment between the VCSEL, the PIN arrays and the mirrors of the waveguide may be readily controlled by simultaneously etching a second cladding or organic layer located on a core or substrate so as to form the waveguide channels and the C4 openings. The C4 openings expose a portion of each pad which is to be electrically connected to the transmitter or receiver chips (Page 8, Paragraph [0031-0033]), in view of which the exact position of the C4s is determined not by the pad but rather by the opening in the second cladding or organic layer printed on the surface of the core. This may be termed a so-called "mask-defined" C4 in its differentiation from a "pad-defined" C4 where the solder joint wets the entire pad. The foregoing may be followed by plating the electronic circuits, filling the channels with waveguide material, and then adding the upper cladding or organic layer (Pages 8 and 9, Paragraphs [0033-0034]). Inasmuch as the mirrors in the waveguide channel and the openings leading to the C4 pads are formed simultaneously, they can be positioned in an extremely precise relationship relative to each other, and at very low and acceptable tolerances (Page 10, Paragraph 0038]).

VI. Grounds of Rejection to be Reviewed

Applicants respectfully request that each of the following grounds be reviewed:

1. Whether Claims 1 and 11 are objectionable due to an informality in the claim language.

2. Whether Claims 1, 8, 11 and 18 are fully anticipated under 35 U.S.C. §102(e) by U.S. Patent No. 6,834,133 B1 (Towle, et al.).

3. Whether Claims 2, 9, 10, 12, 19 and 20 are unpatentable under 35 U.S.C. §103(a) over Towle, et al. and further in view of U.S. Patent Publication No. 2005/0105860 A1 (Oono, et al.).

4. Whether Claims 5-7 and 15-17 are unpatentable under 35 U.S.C. §103(a) over Towle, et al. and further in view of U.S. Publication No. 2002/0084522 A1 (Yoshizawa, et al.).

VII. Argument

A. Objections to Claims 1 and 11 due to informality.

The apparent redundancy which appears in respectively, Line 12 of Claim 1; and Line 12 of Claim 11, arises through an inadvertent typographical error, wherein it should be stated "wherein said at least one transmitter/receiver chip [being] is". However, in its present format, each claim is completely understandable, as recognized by the Examiner, and applicants note that this minor typographical error has no bearing on the patentability or scope of the appealed claims.

B. Rejection Under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,834,133 B1 (Towle, et al.).

1. Claims 1 and 8

The rejections of Claims 1 and 8 under 35 U.S.C. §102(e) should be reversed inasmuch as Towle, et al. fails to disclose the following features:

i) at least one transmitter/receiver chip (20) being coupled to the surface of the second cladding layer (14) (of the opto-electronic package); and

ii) wherein the at least one transmitter/receiver chip (20) is coupled to the surface of the second cladding layer through the interposition of C-4 joins (26).

With regard to Towle, et al., although this patent discloses optical packages and methods of simultaneously optically and electrically coupling an opto-electronic chip to a waveguide substrates distinguishes with regard to the present invention. Towle, et al. is directed to optoelectronic packages and methods to simultaneously couple an optoelectronic chip to a waveguide and substrate using conventional flux soldering processes are disclosed. The disclosed optoelectronic package includes a substrate, a waveguide mounted on the substrate, an optoelectronic chip having electrically conductive contacts

coupled to the substrate via a metallic solder and an optical element located on the optoelectronic chip and coupled to the waveguide via an optical solder which protects the optical element during a metallic soldering of the optoelectronic chip to the substrate.

FIG. 1 of Towle, et al. shows a cross-sectional view of an example optical package 100 prior to assembly. The example optical package 100 includes a substrate 110, a waveguide 112 mounted on the substrate 110, and an optoelectronic chip 114 bonded to the substrate 110. As explained in detail below, the optoelectronic chip 114 includes an optically active area 116 (otherwise known as an optical element) which is optically coupled to the waveguide 112 via an optical solder 118. In the illustrated example, the optical element 116 is bonded to the waveguide 112 via the optical solder 118. The substrate 110 illustrated in FIG. 1 may be implemented by any type of substrate. Thus, the substrate 110 may be formed from any desired type of material. For example, the substrate 110 may be made of an insulative, non-conductive material. The substrate 110 may also have any desired form. In the illustrated example, however, the substrate 10 is made from an Ajinomoto Build-up Film (ABF) dielectric material 120 layered on a substantially general composite substrate 122 and includes a generally planar surface conducive to flip-chip bonding and/or waveguide coupling. By way of a more specific example, the substrate 110 may be implemented by a printed circuit board (PCB) substrate. The PCB may be provided with a chip-bonding surface adapted to mount a flip-chip using flip-chip on board (FCoB) bonding. In such an example, the chip-bonding surface is provided with electrically conductive contacts which are communicatively connected to electrically conductive traces printed on and/or in the PCB substrate.

With regard to the present invention, as set forth in Claims 1 and 8, applicants respectfully note that the Examiner cites Towle, et al. in that it allegedly anticipates these claims. However, contrastingly, the foregoing features i) and ii) in Claims 1 and 11, respectively, provide important advantages over the art, wherein the aspects of the passive alignment of VCSELs to waveguides, which to some general extent are known in the technology, afford a precise alignment of chips relative to an opto-electronic card of a printed circuit board through the intermediary of C4 solder reflow. The improved passive alignment through the intermediary of the structure, as claimed, and the method of combining and producing the components, provides a thermal stability of the opto-electronic card or printed circuit board through the employment of a substrate, which is constituted of a low-expansion material and, thus, accommodates larger VCSELs and pin arrays, as well as facilitating the use of smaller waveguide dimensions. The utilization of the C4s and the solder reflow methods of producing the electronic and electrical interconnections and which are also generally located on different wiring layers and with the waveguides and the adaptability of readily controlling the precision of alignment between the various components and any mirrors of the waveguides

by the use of a second cladding layer or organic layer located in the substrate is used to form the waveguide channels and the C4 openings. The foregoing aspects are not in any manner disclosed in Towle, et al., the latter of which fails to provide the particular type of C4 connections and solder reflow in the structural interrelationship between the various components.

In view of the foregoing, applicants respectfully submit that Claim 1, which describes these particular structural features and the integrated chip with optical inputs and outputs on the cladding layer, as set forth in Claim 8, cannot in any manner be ascertained from Towle, et al., nor are these features considered by the applicants to be obvious to one skilled in the technology. Accordingly, applicants respectfully request that the rejection of Claims 1 and 8 as being anticipated by Towle, et al. be reversed.

2. Claims 11 and 18

The rejection of Claims 11 and 18 as being anticipated by Towle, et al. under 35 U.S.C. §102(e) is also traversed on the basis of the arguments submitted hereinabove with regard to Claims 1 and 8 and wherein applicants note that the method of producing the C4 solder reflow aspects are not in any manner disclosed in Towle, et al. nor are the intended advantages of the present method suggested therein. It remained for the present applicants to set forth the advantages, as described also in connection with Claims 1 and 8, which are equally applicable to the rejection of Claims 11 and 18. On the basis of the foregoing, applicants respectfully request the Board to reverse the rejection of Claims 11 and 18 as being unpatentable over Towle, et al.

C. Rejection Under 35 U.S.C. §103(a), as being unpatentable over Towle, et al. in view of Oono, et al.

1. Claims 2, 9, 10, 12, 19 and 20

Claims 2, 9, 10, 12,19 and 20 have been rejected as being unpatentable over 35 U.S.C. §103(a), over Towle, et al. in view of Oono, et al.

However, applicants note that Oono, et al. fails to provide any of the aspects, as set forth in these particular claims, which are directed to specific property materials, as in Claims 2 and 12; and alignment of VCSELs to waveguides in Claims 9, 10, 19 and 20, wherein the Examiner indicates that Towle, et al. is lacking the particular structural and functional features of these dependent claims, however, Oono, et al. is deemed to suggest the lacking aspect. However, the connections, which are disclosed in Oono, et al., are known in the technology and are not readily combinable by one of skill in the art with the novel features set forth in the present claims in providing for the passive alignment of VCSELs to the waveguides in opto-electronic cards and printed circuit boards in a manner employing the C4 connections and C4 solder reflow aspects. Consequently, even combining Oono, et al. with Towle, et al. fails to disclose the features of the appealed claims, as rejected by the Examiner as

being obvious over the art. The respective materials and alignment aspects between VCSELs and waveguides of the various dependent claims, which are dependent from, respectively, Claims 1 and 11, are deemed to clearly set forth further advantageous and novel features of those particular claims, which are deemed to clearly and patentably distinguish over Towle, et al.

In this connection, applicants refer to a teaching of the Court of Appeals for the Federal Circuit, indicating that "The statutory standard of 103 is whether the invention, considered as a whole, would have been obvious to one skilled in the art, not whether it would have been obvious to one skilled in the art to try various combinations." N.V. Akzo v. E.I. duPont deNemours & Co.,1 USPQ2d 1704, 1707 (Fed Cir. 1987).

Accordingly, in light of the foregoing, it would not be an obvious expedient to combine the features, which the Examiner indicates are lacking in Towle, et al., with the further essentially unrelated aspects of Oono, et al. in order to assert that one skilled in the art would consider these claims to be obvious over the combination of these publications.

In view of the foregoing argument traversing the Examiner's contention that it would be an obvious expedient to combine the features of the Towle, et al. and Oono, et al. patents, the Board is respectfully requested to reverse the Examiner's rejection of these claims under 35 U.S.C. §103(a).

D. Rejection under 35 U.S.C. §103(a), as being unpatentable over Towle, et al. in view of Yoshizawa, et al.

1. Claims 5-7 and 15-17

These claims, which set forth further structural and functional aspects in dependence upon Claims 1 and 11, respectively, are deemed to be obvious by the Examiner over the combination of Towle, et al. and Yoshizawa, et al.

However, applicants note the Examiner indication that although various aspects are lacking in each of the respective publications, these which would be applicable to the invention in that Yoshizawa, et al., when combined with Towle, et al., would render the appealed claims obvious to one skilled in the art. In essence, Yoshizawa, et al. merely discloses an interposer substrate and various through-vias to connect built up layers in a printed circuit board. There is no disclosure of any combination of waveguides and optical components in various chips, including the C4 interconnects, as described and claimed in these dependent appealed claims which have been rejected by the Examiner on the basis that these are allegedly directed to obvious expedients. However, applicants respectfully submit that the Yoshizawa, et al. patent, even if combined with Towle, et al., fails to disclose or suggest the features of these claims, disclosing low expansion materials to minimize strains in C-4 joints, as in Claims 5, 6, 15 and 16, and the index-matched adhesive, as claimed in

Claims 7 and 17, which are dependent from Claims 1 and 11, respectively, and are directed to setting forth further structural and functional details of these claims, and are not at all disclosed in the art of record.

In view of the foregoing, the applicants respectfully request the Board to reverse the rejection of Claims 5-7 and 15-17, as being unpatentable under 35 U.S.C. §103(a) on the basis of the combination of the prior art publications cited by the Examiner.

VIII. Conclusion

Because of the above-discussed distinctions over the references of record, Claims 1, 8, 11 and 18, and Towle, et al. and the advantages associated with these distinctions, these claims are not anticipated by, and patentably distinguish over Towle, et al. Similarly, Claims 2, 5-12 and 15-20 are also deemed to be directed to allowable subject matter by being dependent from , respectively, clearly patentable Claim 1 or Claim 11, and the rejection of these claims, as being unpatentable over Towle, et al., in view of either Oono, et al. or Yoshizawa, et al., is deemed to be improper and the Board is respectfully requested to reverse these rejections.

IX. Claims Appendix

A clean copy of Claims 1, 2, 5-12 and 15-20 is contained in Appendix A to this Appeal Brief.

X. Evidence Appendix

Appellants are not relying on any affidavits, extrinsic documents or extrinsic evidence.

XI. Related Proceedings Appendix

As indicated above, there are no other or pending appeals, interferences or judicial proceedings known to appellants, the appellants' legal representative, or assignee which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Respectfully submitted,

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Enclosure: Appendix A

APPENDIX A

1. An opto-electronic package facilitating the passive alignment of VCSELs to waveguides; said package comprising:

a substrate bearing a first surface;

a first cladding layer positioned on said first surface of said substrate;

a contact pad positioned on at least a position of the surface of said first cladding layer;

a second cladding layer located on a further surface position of said first cladding layer;

a waveguide channel being positioned in said second cladding layer;

optical means being in optical communication with said waveguide channel in said second cladding layer and in electrical connection with said contact pad on said first cladding layer, at least one transmitter/receiver chip being coupled to said surface of said second cladding layer; and

at least one transmitter/receiver chip being coupled to said surface of said second cladding layer through the interposition of C4-joints.

2. An opto-electronic package as claimed in claim 1, wherein said first and second cladding layers are each comprised of an organic material.

Claims 3 and 4 (Cancelled).

5. An opto-electronic package as claimed in claim 1, wherein said substrate comprises a low expansion material approaching the coefficient of thermal expansion of the at least one chip so as to reduce and minimize strains encountered in the C-4 joints.

6. An opto-electronic package as claimed in claim 5, wherein said ~~core~~ substrate material is selected from the group of materials consisting of epoxy glass composites, utilizing thick yarns and low expansion s-glass with a CTE of as low as 10 ppm/°C.

7. An opto-electronic package as claimed in claim 5, wherein an index-matched adhesive couples said second cladding layer directly to said at least one transmitter/receiver chip, and extends between said optical means and waveguide channel.

8. An opto-electronic package as claimed in claim 1, wherein said second cladding layer has an integrated chip with optical inputs and outputs mounted on the surface of said cladding layer.

9. An opto-electronic package as claimed in claim 1, wherein said package comprises a constituent of a printed circuit board providing for the precise alignment of VCSELs to waveguides.

10. An opto-electronic package as claimed in claim 1, wherein said package comprises a constituent of an opto-electronic card providing for the passive alignment of VCSELs to waveguides.

11. A method of producing an opto-electronic package facilitating the passive alignment of VCSELs to waveguides; said method comprising:

providing a ~~core~~ substrate having a first surface;

positioning a first cladding layer on said first surface of said substrate;

arranging a contact pad on at least a portion of the surface of said first cladding layer;

locating a second cladding layer on a further surface portion of said first cladding layer;

positioning a waveguide channel in said second cladding layer;

providing optical means in optical communication with said waveguide channel in said second cladding layer and in electrical connection with said contact pad on said first cladding layer, at least one transmitter/receiver chip being coupled to said surface of said second cladding layer; and

at least one transmitter/receiver chip is coupled to said surface of said second cladding layer through the interposition of C4-joints.

12. A method as claimed in claim 11, wherein said first and second cladding layers are each comprised of an organic material.

Claim 13 and 14 (Cancelled).

15. A method as claimed in claim 11, wherein said ~~core~~ substrate comprises a low expansion material approaching the coefficient of thermal expansion of the at least one chip so as to reduce and minimize strains encountered in the C4 joints.

16. A method as claimed in claim 15, wherein said core material is selected from the group of materials consisting of epoxy glass composites, utilizing thick yarns and low expansion S-glass with a CTE of as low as 10 ppm/°C.

17. A method as claimed in claim 15, wherein an index-matched adhesive couples said second cladding layer directly to said at least one transmitter/receiver chip, and extends between said optical means and waveguide channel.

18. A method as claimed in claim 11, wherein an integrated chip with optical inputs and outputs is mounted on the surface of said second cladding layer.

19. A method as claimed in claim 11, wherein said package comprises a constituent of a printed circuit board providing for the precise alignment of VCSELs to waveguides.

20. A method as claimed in claim 11, wherein said package comprises a constituent of an opto-electronic card providing for the passive alignment of VCSELs to waveguides.